Xuliang Wang

Department of Electronic and Computer Engineering
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ACADEMIC BACKGROUND

Post-Doc. **Tsinghua University**, Beijing, China — 2026
Supervisor: Prof. Xiaosen Liu

Ph.D. **Hong Kong University of Science and Technology**, Hong Kong SAR — 2023
Electronic & Computer Engineering
Supervisor: Prof. Wing-Hung Ki
Thesis: IR-Drop- and Timing-Aware Power Management Techniques for Microprocessors

B.S. **Southeast University**, Nanjing, China — 2018
Electronic Engineering

RESEARCH INTERESTS & VISION

My research focuses on mixed-signal power management IC (PMIC) design, seamlessly integrated with 2.5D/3D advanced packaging. My vision is to pioneer ultra-high-density, energy-efficient power delivery and mixed-signal architectures for next-generation AI computing, edge-intelligence, and resilient semiconductor systems.

Pillar 1: Integrated Power Delivery for 2.5D/3D Heterogeneous System

- Vertical Power Delivery (VPD) & System-in-Package (SiP): Architectures for chiplet systems, including high-density Intermediate Bus Converters (IBC) and Point-of-Load (PoL) regulators tailored for 2.5D/3D integration.
- Integrated Voltage Regulators (IVR): Multiphase package-integrated regulators and flip-chip PMICs optimized for granular power distribution in AI accelerators and data centers.
- Holistic Circuit-Package Co-Design: Systematic optimization framework and design trade-offs to push the Pareto frontier towards higher volumetric power density and system efficiency.

Pillar 2: High-Efficiency Power Conversion & Intelligent Mixed-Signal Control

- Hybrid Topology Innovation: Advanced Hybrid/Resonant Switched-Capacitor (SC) topologies for soft-switching high-density regulation and inherently balanced multiphase DC-DC converters.
- Intelligent Control Algorithms: Circuit-level implementation of model/learning-based control, digital control, and transient-aware algorithms for rapid load tracking.
- Multi-Output & Cross-Regulation Mitigation: Single-Inductor Multiple-Output (SIMO) architectures with active cross-regulation suppression for compact systems.

Pillar 3: Clocking-Power Co-Design, Dynamic Scaling & Resilient Architectures

- Unified Power-Clock Regulation & DVFS: Instruction-driven adaptive clocking, Unified Voltage-and-Frequency Regulators (UVFRs), and Minimum Energy Point (MEP) tracking for Ultra-Low Power (ULP) edge devices.
- Domain-Specific & Emerging Computing Support: Power-timing co-design for In-Memory Computing (IMC) architectures, voltage-stacked power delivery, and Wireless Power Transfer (WPT) for autonomous systems.
- Hardware Security at Circuit Level: Integrated countermeasure techniques for Power Side-Channel Attack.

SELECTED RESEARCH ACHIEVEMENTS

Pillar 1: Integrated Power Delivery for 2.5D/3D Heterogeneous System

- Proven Tape-out Track Record: Independently spearheaded the end-to-end design, tape-out, and experimental validation of **7** flip-chip Power Management ICs (PMICs), alongside co-designing and verifying 4 additional PMICs, maintaining a **100%** silicon success rate across all projects.
- Methodology Leadership in System-in-Package (SiP): Established an end-to-end design methodology for Flip-chip PMICs and SiP integration, targeting the reduction of iteration cycles for complex multi-chiplet power delivery networks.
- Premier Solid-State Venue Impact: First-authored **3** flagship conference papers at *IEEE CICC 2026* and *IEEE ESSERC 2026*. First-authored **2** regular papers in the flagship ***IEEE Journal of Solid-State Circuits (JSSC)*** focusing on advanced IVR architectures.

Pillar 2: High-Efficiency Power Conversion & Intelligent Mixed-Signal Control

- Architectural & Topology Breakthroughs: Pioneered the development of novel Hybrid/Resonant Switched-Capacitor (SC) topologies and trajectory-based soft-switching control, continually pushing the Pareto frontiers of volumetric power density and system efficiency.
- Domain-Specific Power Management: Pioneering the chip implementation of a lightweight learning algorithm into SIMO converter control, achieving dynamic, real-time cross-regulation mitigation in heterogeneous SoC.
- Power Electronics Track Record: Published **5** first-authored papers in premier forums, including *IEEE Applied Power Electronics Conference & Exposition (APEC)* and *IEEE Workshop on Control & Modeling for Power Electronics (COMPEL)*, demonstrating sustained leadership in high-density power conversion.

Pillar 3: Clocking-Power Co-Design, Dynamic Scaling & Resilient Architectures

- Proactive Power-Performance Scaling: Spearheaded research on instruction-driven proactive clocking and adaptive power management, achieving significant energy savings and ultra-dynamic transient response.
- Unified Power-and-Clock Regulation: Led the design of unified voltage-and-frequency regulators (UVFR) for energy-efficient computing, bridging the gap between digital clocking and analog power delivery.
- Top-Tier Publication Success: Published **4** first-authored papers, highlighted by a regular paper in ***IEEE Transactions on Circuits and Systems I (TCAS-I)*** and *IEEE A-SSCC 2022.*

HONORS & ACADEMIC SERVICE

2026	Session Chair – *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*
2026	Journal Reviewer – *IEEE Transactions on Power Electronics (TPEL)*
2023-2025	Beijing Municipal Natural Science Foundation – Youth Fund (Grant No. 4244106)
2023-2026	National Program for Recruiting Overseas Postdoctoral Talent
2023-2026	Shuimu Tsinghua Scholarship (Global Recruitment)

PROFESSIONAL EXPERIENCE

Post-Doctoral Fellow	**2023-2026**	**School of Integrated Circuits, Tsinghua University**
Assistant Research Fellow	**2023-2026**	**School of Integrated Circuits, Tsinghua University**
Teaching Assistant	**2018-2023**	**Hong Kong University of Science and Technology**

CONFERENCE PAPERS

[C1] **X. Wang**, Z. Liu, H. Wang, T. Min, W.-H. Ki, Y. Wang, and X. Liu, "Mobius: A 12V-to-1V Charge-Cross-Converging Converter Ring with Monolithic Handshake Driving for Next-Generation AI Server," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C2] **X. Wang**, Z. Liu, Y. Yao, W. Wu, J. Jiang, Y. Wang, and X. Liu, "A 96.6%-Peak-Efficiency 4.63-A/mm^3-Peak-Density Resonant-Tank Converter with RDL Trace Inductor and Trajectory Control for Vertical Power Delivery," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C3] R. Chen, X. Men, Z. Liu, Y. Wang, **X. Wang**, J. Xu, J. Yu, R. Chen, J. Wei, … "An Autonomous Computational Current-Booster Chiplet for Fast Droop Mitigation and Universal Compatibility in 3D-IC Vertical Power Delivery," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C4] X. Men, R. Chen, Y. Wang, B. Zhang, Z. Liu, H. Liu, **X. Wang**, Z. Zhang, J. Yu, … "A 280 MHz All-Digital Current-Mode IVR with Dual-Observation Current Telemetry and Kalman Filter-Based Fusion for Scalable Ganged Systems," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C5] W. Wu, X. Bao, J. Wang, S. Chen, **X. Wang**, X. Liu, Y. Wang, and L. Zhang, "A 256-316-GHz Frequency Quadrupler with Polyphase Continuous Harmonic Tuning and Power Combining Network in 65-nm CMOS," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C6] **X. Wang**, W.-H. Ki, Y. Liu, J. Wei, Y. Wang, and X. Liu, "Geometrical State-Plane Analysis of GaN-Based Buck Converters with Auxiliary-Assisted Zero-Voltage Switching," in *Proc. IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jul. 2026 (Accepted as Lecture).

[C7] **X. Wang**, W.-H. Ki, Y. Yao, Y. Zhong, Y. Wang, and X. Liu, "Algebraic Synthesis for A Family of Inherently Balanced Multi-Phase Hybrid Switched-Capacitor Converters Leveraging Cyclic Symmetry," in *Proc. IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jul. 2026 (Accepted as Poster).

[C8] **X. Wang**, H. Wang, X. Men, R. Chen, J. Jiang, Y. Wang, and X. Liu, "Unicorn: A Unified Clock-and-Power SoC with RL-Adapted Digital SIMO Control and In-TRO Frequency Boosting for Edge Computing," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2026, pp. 1-4.

[C9] Y. Liu, Y. Yao, G. Zhu, D. Pan, C. Hua, **X. Wang**, W. Xu, Y. Li, W.-H. Ki, L. Cheng, and Z. Zhu, "A 200kHz Self-Powered Isolated Gate Driver for SiC and IGBT with Synchronous Regulation of 62.6% Efficiency," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2026, pp. 1-4.

[C10] **X. Wang**, H. Wang, Z. Liu, Y. Yao, Y. Liu, W.-H. Ki, J. Wei, Y. Wang, and X. Liu, "X-ReLA: a Family of Stacked-Ladder Charge-Cross-Converging ReSC with 98.2% Peak Efficiency Featuring Wide Voltage Conversion Ratio and Always Reduced Inductor Current," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 3314-3320.

[C11] **X. Wang**, H. Wang, Z. Liu, Y. Yao, Y. Liu, W.-H. Ki, J. Wei, Y. Wang, and X. Liu, "A Multi-Resonant Cascaded Series-Parallel Switched-Capacitor Converter Featuring Continuously Scalable Conversion Ratio," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 2097-2103.

[C12] H. Wang, Z. Liu, J. Xu, **X. Wang**, Y. Liu, X. Li, J. Cui, Y. Wang, and X. Liu, "A 30-60V Input 6V Output Regulated Resonant SC Converter with Unified Hard-Soft Switching Control Achieving 100A and 1339W/in^3 for High-Performance Computing," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 1693-1699.

[C13] H. Wang, Z. Liu, J. Xu, **X. Wang**, M. Xiong, Y. Liu, X. Li, J. Cui, Y. Wang, and X. Liu, "Current–Temperature–Resistance Modeling and Conversion Loss Sharing Methodology for Optimized Efficiency and Thermal Distribution in Large-Scale HPC Power Delivery Networks," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 1216-1221.

[C14] H. Wang, Z. Liu, J. Xu, **X. Wang**, M. Xiong, Y. Liu, X. Li, J. Cui, Y. Wang, X. Liu, "A 1295W/in^3 160A Quad-Phase VPD Module with Flexible Ganging and Multiphysics Optimization for Large-Scale HPC Systems," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 1060-1066.

[C15] R. Chen, Z. Liu, X. Men, **X. Wang**, Y. Wang, X. Liu, "A Triple-Path Resonant-Tracked Voltage Regulator with Package Inductor for System-on-Wafer Vertical Power Delivery," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May. 2026, pp. 93-96.

[C16] X. Sun, **X. Wang**, R. Chen, X. Men, J. Jiang, Y. Wang, and X. Liu, "A 10W 3.8-5V Input IVR Chiplet with 93%-Peak-Efficiency and 3.2A/mm^2 Density Featuring Wide Load Range and Adaptive Ganging for 2.5D/3D Vertical Power Delivery," in *Proc. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Jun. 2025, pp. 1-3.

[C17] F. Tian, J. Chen, K. Shao, Z. Liu, J. Zheng, H. Wu, C. Fang, X. Wang, Z. Shen, P. Dong, Y. Yao, **X. Wang**, J. Yang, M. Sawan, C.-Y. Tsui, and K.-T. Cheng, "E-NPU: A 34~126nJ/Class Event-Driven Adaptive Neural SoC with Signal-Dynamics-Aware Feature Clustering and Multi-Model In-Memory Inference/Training for Personalized Medical Wearables," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2025, pp. 1-3.

[C18] **X. Wang**, H. Wang, Y. Liu, Y. Wang, B. Zhang, H. Liu, Y. Wang, and X. Liu, "Concurrent Charge Distribution and Time-Optimal Control for Unordered Single-Inductor Dual-Output Converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2025, pp. 2675-2680.

[C19] H. Wang, **X. Wang**, Y. Wang, and X. Liu, "A 660W, 96% Efficiency 3D Heterogeneously Integrated Digital DC/DC Power Module for Vertical Power Delivery," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2025, pp. 1544-1550.

[C20] H. Wang, **X. Wang**, Y. Wang, and X. Liu, "Evaluation Index-Based Multiphysics Coupling Model and Analysis Methodology for High-Reliable Power Supply Module," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2025, pp. 2556-2561.

[C21] H. Zhang, C. Wang, X. Liu, **X. Wang**, R. Chen, X. Men, F. Wang, and Y. Wang, "A Discontinuously Resonant Operation for Continuously-Scalable-Conversion-Ratio Switched Capacitor Converter with Enhanced Power Efficiency and Output Capability," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Oct. 2025, pp. 1-5.

[C22] Y. Wang, **X. Wang**, B. Zhang, R. Chen, X. Men and X. Liu, "A Capacitorless Fully Synthesizable Digital-LDO Using Scalable APR-Friendly Power MOS Cell with 13.71A/mm^2 Current Density," in *Proc. IEEE International Conference on Electron Devices and Solid-State Circuits (EDSS)*, Jun. 2025, pp. 500-501.

[C23] X. Sun, J. Yu, **X. Wang**, J. Wei, J. Jiang, C. Zhan, Y. Wang, and X. Liu, "A 92%-Efficiency 0.828μs Settling Time FC5L Voltage Regulator Featuring Time-Domain Charge Balancing & Flying Capacitor Self-Switching for Wide Dynamic Range & Fast Transient Chiplet Applications," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2024, pp. 1-2.

[C24] **X. Wang**, W.-H. Ki, and P. K. T. Mok, "A Self-Clocked TDC-Based Unified Clock and Voltage Regulator with Replica Frequency-Locked Loop and Hysteresis Switching in 65nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2022, pp. 1-3.

[C25] **X. Wang** and W.-H. Ki, "Partitioning Scheme and Performance Analysis of Distributed Digital Low-Dropout Regulators in SoC," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, Jun. 2022, pp. 2520-2524**.**

[C26] **X. Wang** and W.-H. Ki, "A 65-nm Clock-Domain-Crossing Controller for Digital LDO Regulator with 1.7-ns Response Time," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Nov. 2022, pp. 284-288**.**

JOURNAL PAPERS

[J1] **X. Wang**, X. Liu, and W.-H. Ki, "A Self-Clocked and Variation-Tolerant Unified Voltage-and-Frequency Regulator for In-Order Executed Digital Loads," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, issue 11, pp. 4627-4640, Nov. 2023**.**

[J2] **X. Wang**, R. Chen, H. Wang, Y. Liu, W.-H. Ki, Y. Wang, and X. Liu, "A 0.73 A/mm^3 Switched-Capacitor-Stack-Inductor Volumetric Integrated Voltage Regulator with Auxiliary-Assisted Gain Boosting for High-Density PoL Applications," *IEEE Journal of Solid-State Circuits* (Early Access)**.**

[J3] **X. Wang**, X. Men, Z. Liu, W.-H. Ki, J. Wei, Y. Wang, and X. Liu, "A 6-A 93.8%-Peak-Efficiency 5V-to-Sub-1V Segment-Interlaced SC-Parallel-Inductor Converter Featuring Inherently Balanced Ganging for Wafer-Scale Computing System," *IEEE Journal of Solid-State Circuits* (Early Access)**.**

TECHNICAL APPENDIX: CHIP & PROTOTYPE GALLERY

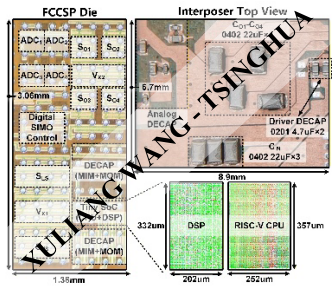

Figure 1 Unicorn [CICC 2026]

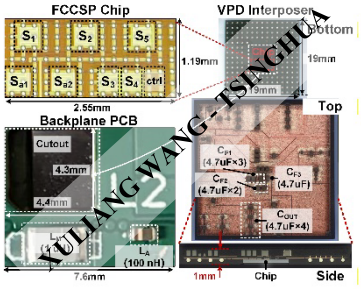

Figure 2 SCSL [JSSC 2026]

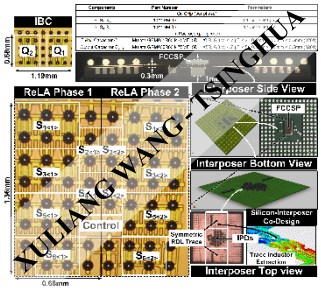

Figure 3 ReLA [ESSERC 2026]

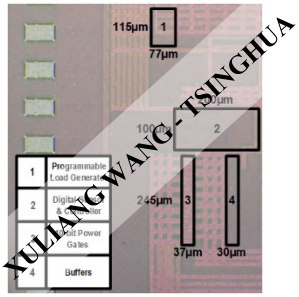

Figure 4 UVFR [TCAS-I 2023]

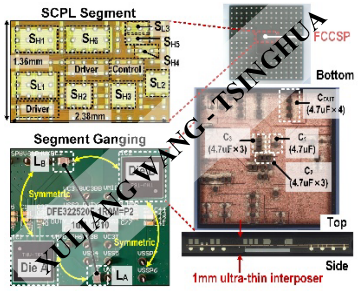

Figure 5 SI-SCPL [JSSC 2026]

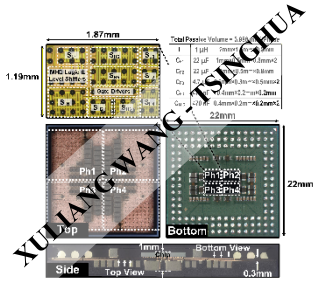

Figure 6 Mobius [ESSERC 2026]