Xuliang Wang

Department of Electronic and Computer Engineering, PowerSAC
Post-Doctoral Fellow — The Hong Kong University of Science and Technology, Hong Kong SAR
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ACADEMIC BACKGROUND

Post-Doc.	**The Hong Kong University of Science and Technology**, Hong Kong SAR *Supervisor:* Chair Prof. Kevin Jing Chen (*IEEE Fellow, PowerSAC Director*)	Present
Post-Doc.	**Tsinghua University**, Beijing, China *Supervisor:* Prof. Xiaosen Liu	2026
Ph.D.	**The Hong Kong University of Science and Technology**, Hong Kong SAR Electronic & Computer Engineering *Supervisor:* Prof. Wing-Hung Ki *Thesis: IR-Drop- and Timing-Aware Power Management Techniques for Microprocessors*	2023
B.S.	**Southeast University**, Nanjing, China Electronic Engineering	2018

RESEARCH INTERESTS & VISION

My research focuses on mixed-signal power management IC (PMIC) design, seamlessly integrated with 2.5D/3D advanced packaging. My vision is to pioneer ultra-high-density, energy-efficient power delivery and mixed-signal architectures for next-generation AI computing, edge intelligence, and resilient semiconductor systems.

Pillar 1: Integrated Power Delivery for 2.5D/3D Heterogeneous System

- Vertical Power Delivery (VPD) & System-in-Package (SiP): Architectures for chiplet systems, including high-density Intermediate Bus Converters (IBC) and Point-of-Load (PoL) regulators tailored for 2.5D/3D integration.
- Integrated Voltage Regulators (IVR): Multiphase package-integrated regulators and flip-chip PMICs optimized for granular power distribution in AI accelerators and data centers.
- Holistic Circuit-Package Co-Design: Systematic optimization framework and design trade-offs to push the Pareto frontier towards higher volumetric power density and system efficiency.

Pillar 2: High-Efficiency Power Conversion & Intelligent Mixed-Signal Control

- Hybrid Topology Innovation: Advanced Hybrid/Resonant Switched-Capacitor (SC) topologies for soft-switching high-density regulation and inherently balanced multiphase DC-DC converters.
- Intelligent Control Algorithms: Circuit-level implementation of model/learning-based control, digital control, and transient-aware algorithms for rapid load tracking.
- Multi-Output & Cross-Regulation Mitigation: Single-Inductor Multiple-Output (SIMO) architectures with active cross-regulation suppression for compact systems.

Pillar 3: Clocking-Power Co-Design, Dynamic Scaling & Resilient Architectures

- Unified Power-Clock Regulation & DVFS: Instruction-driven adaptive clocking, Unified Voltage-and-Frequency Regulators (UVFRs), and Minimum Energy Point (MEP) tracking for Ultra-Low Power (ULP) edge devices.
- Domain-Specific & Emerging Computing Support: Power-timing co-design for In-Memory Computing (IMC) architectures, voltage-stacked power delivery, and Wireless Power Transfer (WPT) for autonomous systems.

- Hardware Security at Circuit Level: Integrated countermeasure techniques for Power Side-Channel Attack.

SELECTED RESEARCH ACHIEVEMENTS

Pillar 1: Integrated Power Delivery for 2.5D/3D Heterogeneous System

- Proven Tape-out Track Record: Independently spearheaded the end-to-end design, tape-out, and experimental validation of **7** flip-chip Power Management ICs (PMICs), alongside co-designing and verifying 4 additional PMICs, maintaining a **100%** silicon success rate across all projects.
- Methodology Leadership in System-in-Package (SiP): Established an end-to-end design methodology for Flip-chip PMICs and SiP integration, targeting the reduction of iteration cycles for complex multi-chiplet power delivery networks.
- Premier Solid-State Venue Impact: First-authored **3** flagship conference papers at *IEEE CICC 2026* and *IEEE ESSERC 2026*. First-authored **2** regular papers in the ***IEEE Journal of Solid-State Circuits (JSSC)*** focusing on advanced IVR architectures.

Pillar 2: High-Efficiency Power Conversion & Intelligent Mixed-Signal Control

- Architectural & Topology Breakthroughs: Pioneered the development of novel Hybrid/Resonant Switched-Capacitor (SC) topologies and trajectory-based soft-switching control, continually pushing the Pareto frontiers of volumetric power density and system efficiency.
- Domain-Specific Power Management: Pioneering the chip implementation of a lightweight learning algorithm into SIMO converter control, achieving dynamic, real-time cross-regulation mitigation in heterogeneous SoC.
- Power Electronics Track Record: Published **6** first-authored papers in premier conferences, including *IEEE Applied Power Electronics Conference & Exposition (APEC)* and *IEEE Workshop on Control & Modeling for Power Electronics (COMPEL)*, demonstrating sustained leadership in high-density power conversion.

Pillar 3: Clocking-Power Co-Design, Dynamic Scaling & Resilient Architectures

- Proactive Power-Performance Scaling: Spearheaded research on instruction-driven proactive clocking and adaptive power management, achieving significant energy savings and ultra-dynamic transient response.
- Unified Power-and-Clock Regulation: Led the design of unified voltage-and-frequency regulators (UVFR) for energy-efficient computing, bridging the gap between digital clocking and analog power delivery.
- Top-Tier Publication Success: Published **4** first-authored papers, highlighted by a regular paper in ***IEEE Transactions on Circuits and Systems I (TCAS-I)*** and *IEEE A-SSCC 2022.*

HONORS & ACADEMIC SERVICE

2026	**Session Chair** – *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*
2026	Journal Reviewer – *IEEE Transactions on Power Electronics (TPEL)*
2023-2025	**Principal Investigator** – Beijing Municipal Natural Science Foundation (Grant No. 4244106)
2023-2026	Key Participant – National Natural Science Foundation of China (Grant No. 62374100)
2023-2026	Key Participant – National Key R&D Program of China (Grant No. 2022YFB4401100)
2026	Key Participant – Beijing National Research Center for Information Science and Technology (Grant No. BNR2026RC01013)
2023-2026	National Program for Recruiting Overseas Postdoctoral Talent
2023-2026	Shuimu Tsinghua Scholarship (Global Recruitment)

PROFESSIONAL EXPERIENCE

Post-Doctoral Fellow	**2026-Present**	**The Hong Kong University of Science and Technology**
Post-Doctoral Fellow	**2023-2026**	**School of Integrated Circuits, Tsinghua University**
Assistant Research Fellow	**2023-2026**	**School of Integrated Circuits, Tsinghua University**
Teaching Assistant	**2018-2023**	**The Hong Kong University of Science and Technology**

CONFERENCE PAPERS

[C1] **X. Wang**, T. Min, X. Liu, and K. J. Chen, "Octopus: a 5-mm-Height 337-W/in^3 Resonant Converter Ring Featuring Saturation-Free Magnetic Flux and Reduced Resonant Capacitor Ripple via Quad-Phase Coupled Inductors," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2027 (Accepted as Lecture).

[C2] **X. Wang**, Z. Liu, H. Wang, T. Min, W.-H. Ki, Y. Wang, and X. Liu, "Mobius: A 12V-to-1V Charge-Cross-Converging Converter Ring with Monolithic Handshake Driving for Next-Generation AI Server," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C3] **X. Wang**, Z. Liu, Y. Yao, W. Wu, J. Jiang, Y. Wang, and X. Liu, "A 96.6%-Peak-Efficiency 4.63-A/mm^3-Peak-Density Resonant-Tank Converter with RDL Trace Inductor and Trajectory Control for Vertical Power Delivery," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C4] R. Chen, X. Men, Z. Liu, Y. Wang, **X. Wang**, J. Xu, J. Yu, R. Chen, J. Wei, … "An Autonomous Computational Current-Booster Chiplet for Fast Droop Mitigation and Universal Compatibility in 3D-IC Vertical Power Delivery," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C5] X. Men, R. Chen, Y. Wang, B. Zhang, Z. Liu, H. Liu, **X. Wang**, Z. Zhang, J. Yu, … "A 280 MHz All-Digital Current-Mode IVR with Dual-Observation Current Telemetry and Kalman Filter-Based Fusion for Scalable Ganged Systems," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C6] W. Wu, X. Bao, J. Wang, S. Chen, **X. Wang**, X. Liu, Y. Wang, and L. Zhang, "A 256-316-GHz Frequency Quadrupler with Polyphase Continuous Harmonic Tuning and Power Combining Network in 65-nm CMOS," in *Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sept. 2026, pp. 1-4 (Accepted as Lecture).

[C7] **X. Wang**, W.-H. Ki, Y. Liu, J. Wei, Y. Wang, and X. Liu, "Geometrical State-Plane Analysis of GaN-Based Buck Converters with Auxiliary-Assisted Zero-Voltage Switching," in *Proc. IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jul. 2026 (Accepted as Lecture).

[C8] **X. Wang**, W.-H. Ki, Y. Yao, Y. Zhong, Y. Wang, and X. Liu, "Algebraic Synthesis for A Family of Inherently Balanced Multi-Phase Hybrid Switched-Capacitor Converters Leveraging Cyclic Symmetry," in *Proc. IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jul. 2026 (Accepted as Poster).

[C9] **X. Wang**, H. Wang, X. Men, R. Chen, J. Jiang, Y. Wang, and X. Liu, "Unicorn: A Unified Clock-and-Power SoC with RL-Adapted Digital SIMO Control and In-TRO Frequency Boosting for Edge Computing," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2026, pp. 1-4.

[C10] Y. Liu, Y. Yao, G. Zhu, D. Pan, C. Hua, **X. Wang**, W. Xu, Y. Li, W.-H. Ki, L. Cheng, and Z. Zhu, "A 200kHz Self-Powered Isolated Gate Driver for SiC and IGBT with Synchronous Regulation of 62.6% Efficiency," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2026, pp. 1-4.

[C11] **X. Wang**, H. Wang, Z. Liu, Y. Yao, Y. Liu, W.-H. Ki, J. Wei, Y. Wang, and X. Liu, "X-ReLA: a Family of Stacked-Ladder Charge-Cross-Converging ReSC with 98.2% Peak Efficiency Featuring Wide Voltage Conversion Ratio and Always Reduced Inductor Current," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 3314-3320.

[C12] **X. Wang**, H. Wang, Z. Liu, Y. Yao, Y. Liu, W.-H. Ki, J. Wei, Y. Wang, and X. Liu, "A Multi-Resonant Cascaded Series-Parallel Switched-Capacitor Converter Featuring Continuously Scalable Conversion Ratio," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 2097-2103.

[C13] H. Wang, Z. Liu, J. Xu, **X. Wang**, Y. Liu, X. Li, J. Cui, Y. Wang, and X. Liu, "A 30-60V Input 6V Output Regulated Resonant SC Converter with Unified Hard-Soft Switching Control Achieving 100A and 1339W/in^3 for High-Performance Computing," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 1693-1699.

[C14] H. Wang, Z. Liu, J. Xu, **X. Wang**, M. Xiong, Y. Liu, X. Li, J. Cui, Y. Wang, and X. Liu, "Current–Temperature–Resistance Modeling and Conversion Loss Sharing Methodology for Optimized Efficiency and Thermal Distribution in Large-Scale HPC Power Delivery Networks," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 1216-1221.

[C15] H. Wang, Z. Liu, J. Xu, **X. Wang**, M. Xiong, Y. Liu, X. Li, J. Cui, Y. Wang, X. Liu, "A 1295W/in^3 160A Quad-Phase VPD Module with Flexible Ganging and Multiphysics Optimization for Large-Scale HPC Systems," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2026, pp. 1060-1066.

[C16] R. Chen, Z. Liu, X. Men, **X. Wang**, Y. Wang, X. Liu, "A Triple-Path Resonant-Tracked Voltage Regulator with Package Inductor for System-on-Wafer Vertical Power Delivery," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May. 2026, pp. 93-96.

[C17] X. Sun, **X. Wang**, R. Chen, X. Men, J. Jiang, Y. Wang, and X. Liu, "A 10W 3.8-5V Input IVR Chiplet with 93%-Peak-Efficiency and 3.2A/mm^2 Density Featuring Wide Load Range and Adaptive Ganging for 2.5D/3D Vertical Power Delivery," in *Proc. IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Jun. 2025, pp. 1-3.

[C18] F. Tian, J. Chen, K. Shao, Z. Liu, J. Zheng, H. Wu, C. Fang, X. Wang, Z. Shen, P. Dong, Y. Yao, **X. Wang**, J. Yang, M. Sawan, C.-Y. Tsui, and K.-T. Cheng, "E-NPU: A 34~126nJ/Class Event-Driven Adaptive Neural SoC with Signal-Dynamics-Aware Feature Clustering and Multi-Model In-Memory Inference/Training for Personalized Medical Wearables," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2025, pp. 1-3.

[C19] **X. Wang**, H. Wang, Y. Liu, Y. Wang, B. Zhang, H. Liu, Y. Wang, and X. Liu, "Concurrent Charge Distribution and Time-Optimal Control for Unordered Single-Inductor Dual-Output Converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2025, pp. 2675-2680.

[C20] H. Wang, **X. Wang**, Y. Wang, and X. Liu, "A 660W, 96% Efficiency 3D Heterogeneously Integrated Digital DC/DC Power Module for Vertical Power Delivery," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2025, pp. 1544-1550.

[C21] H. Wang, **X. Wang**, Y. Wang, and X. Liu, "Evaluation Index-Based Multiphysics Coupling Model and Analysis Methodology for High-Reliable Power Supply Module," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2025, pp. 2556-2561.

[C22] H. Zhang, C. Wang, X. Liu, **X. Wang**, R. Chen, X. Men, F. Wang, and Y. Wang, "A Discontinuously Resonant Operation for Continuously-Scalable-Conversion-Ratio Switched Capacitor Converter with Enhanced Power Efficiency and Output Capability," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Oct. 2025, pp. 1-5.

[C23] Y. Wang, **X. Wang**, B. Zhang, R. Chen, X. Men and X. Liu, "A Capacitorless Fully Synthesizable Digital-LDO Using Scalable APR-Friendly Power MOS Cell with 13.71A/mm^2 Current Density," in *Proc. IEEE International Conference on Electron Devices and Solid-State Circuits (EDSS)*, Jun. 2025, pp. 500-501.

[C24] X. Sun, J. Yu, **X. Wang**, J. Wei, J. Jiang, C. Zhan, Y. Wang, and X. Liu, "A 92%-Efficiency 0.828μs Settling Time FC5L Voltage Regulator Featuring Time-Domain Charge Balancing & Flying Capacitor Self-Switching for Wide Dynamic Range & Fast Transient Chiplet Applications," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2024, pp. 1-2.

[C25] **X. Wang**, W.-H. Ki, and P. K. T. Mok, "A Self-Clocked TDC-Based Unified Clock and Voltage Regulator with Replica Frequency-Locked Loop and Hysteresis Switching in 65nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2022, pp. 1-3.

[C26] **X. Wang** and W.-H. Ki, "Partitioning Scheme and Performance Analysis of Distributed Digital Low-Dropout Regulators in SoC," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, Jun. 2022, pp. 2520-2524**.**

[C27] **X. Wang** and W.-H. Ki, "A 65-nm Clock-Domain-Crossing Controller for Digital LDO Regulator with 1.7-ns Response Time," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Nov. 2022, pp. 284-288**.**

JOURNAL PAPERS

[J1] **X. Wang**, X. Liu, and W.-H. Ki, "A Self-Clocked and Variation-Tolerant Unified Voltage-and-Frequency Regulator for In-Order Executed Digital Loads," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, issue 11, pp. 4627-4640, Nov. 2023**.**

[J2] **X. Wang**, R. Chen, H. Wang, Y. Liu, W.-H. Ki, Y. Wang, and X. Liu, "A 0.73 A/mm^3 Switched-Capacitor-Stack-Inductor Volumetric Integrated Voltage Regulator with Auxiliary-Assisted Gain Boosting for High-Density PoL Applications," *IEEE Journal of Solid-State Circuits*, vol. 61, no. 10, pp. 5825-5837, Oct. 2026**.**

[J3] **X. Wang**, X. Men, Z. Liu, W.-H. Ki, J. Wei, Y. Wang, and X. Liu, "A 6-A 93.8%-Peak-Efficiency 5V-to-Sub-1V Segment-Interlaced SC-Parallel-Inductor Converter Featuring Inherently Balanced Ganging for Wafer-Scale Computing System," *IEEE Journal of Solid-State Circuits* (Early Access)**.**

[J4] H. Wang, **X. Wang**, Y. Liu, and X. Liu, "Design and Load-Adaptive Hybrid Control of a Quarter Brick R²SC Converter for Data Center Power Delivery," *IEEE Transactions on Industrial Electronics* (Revision 1).

[J5] R. Chen, Z. Liu, X. Men, **X. Wang**, Y. Wang, W. Zhang, J. Yu, and X. Liu, "A Triple-Path Resonance-Tracking Voltage Regulator Chiplet with Package Inductor for System-on-Wafer Vertical Power Delivery," *IEEE Transactions on Power Electronics* (Revision 1).

[J6] **X. Wang**, T. Min, J. Ma, Y. Yu, X. Liu, and K. J. Chen, "Reduced-Order Control of Heterogeneous DC-DC Converters via Physical Graph Topology," *IEEE Control Systems Letters* (Joint Submission to ACC).

TECHNICAL APPENDIX: CHIP & PROTOTYPE GALLERY

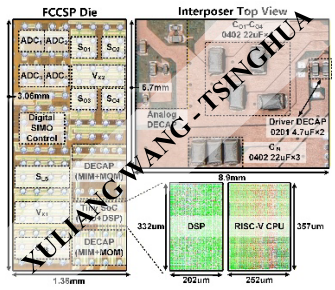


Figure 1 Unicorn [CICC 2026]

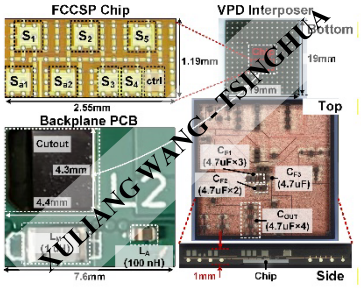


Figure 2 SCSL [JSSC 2026]

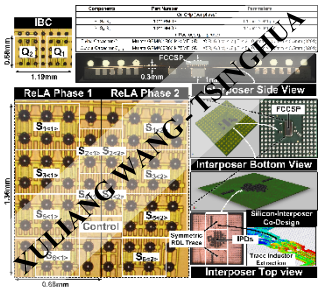


Figure 3 ReLA [ESSERC 2026]

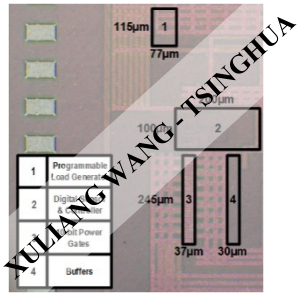


Figure 4 UVFR [TCAS-I 2023]

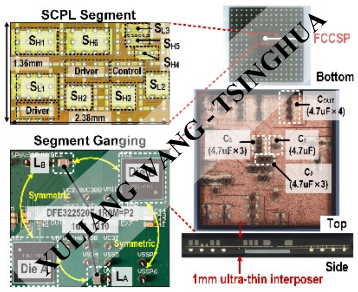


Figure 5 SI-SCPL [JSSC 2026]

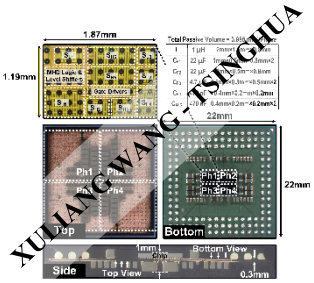


Figure 6 Mobius [ESSERC 2026]

王旭亮

电子及计算机工程、功率半导体与应用中心(PowerSAC)
博士后研究员 香港科技大学, 香港
邮箱: xwangef@connect.ust.hk 个人网站: Xuliang Wang — VLSI & Power Management

学术背景

博士后 **香港科技大学**，香港 至今
导师: 陈敬讲席教授（*IEEE Fellow, PowerSAC 主任*）

博士后 **清华大学**，北京，中国 2026
导师: 刘效森副教授

博士 **香港科技大学**，香港 2023
电子及计算机工程
导师: 暨永雄教授（荣休）
毕业论文: ***IR-Drop- and Timing-Aware Power Management Techniques for Microprocessors***

本科 **东南大学**，南京，中国 2018
电子科学与技术

研究兴趣与愿景

我的研究重点是混合信号电源管理集成电路（PMIC）设计，并将其与 2.5D/3D 先进封装技术无缝衔接。我的愿景是研发超高密度、高能效的电源传输和混合信号架构，以应用于下一代人工智能计算、边缘智能和高可靠性半导体系统，具体围绕三个相互关联、相互促进的研究支柱展开：

支柱一：面向 2.5D/3D 异构系统的集成供电

- 垂直电源传输 (VPD) 和系统级封装 (SiP)：芯片系统架构，包括高密度中间总线转换器 (IBC) 和负载点 (PoL) 稳压器，专为 2.5D/3D 集成量身定制。
- 集成电压调节器 (IVR)：多相封装集成调节器和倒封装 PMIC，针对 AI 加速器和数据中心进行精细电源分配。
- 电路封装协同设计：系统化的优化框架和设计权衡，以推动帕累托前沿向更高的 3D 功率密度和系统效率迈进。

第二支柱：高效功率转换和智能混合信号控制

- 混合拓扑创新：先进的混合/谐振开关电容 (Switched Capacitor, SC) 拓扑，用于软开关高密度电压调节和自主平衡的多相 DC-DC 转换器。
- 智能控制算法：基于模型/强化学习的控制、数字控制和瞬态感知算法的电路级实现，用于快速负载跟踪。
- 多输出和交叉调节抑制：具有主动交叉调节抑制的单电感多输出 (SIMO) 架构，适用于紧凑型系统。

第三支柱：时钟功耗协同设计、动态扩展和弹性架构

- 统一电源时钟调节和 DVFS: 指令驱动的自适应时钟、统一电压和频率调节器 (UVFR) 以及用于超低功耗 (ULP) 边缘设备的最小能量点 (MEP) 跟踪。
- 专用领域和新兴计算支持：内存计算架构的电源时序协同设计、电压堆叠供电和自主系统的无线电力传输。
- 电路级硬件安全：针对电源侧信道攻击的集成对抗技术。

代表性科研成果

支柱一：面向 2.5D/3D 异构系统的集成供电

- 成熟的流片经验：独立主导了 **7** 款倒装芯片电源管理 IC (PMIC) 的端到端设计、流片和实验验证，同时参与了另外 **4** 款 PMIC 的设计和验证，所有项目均保持 **100%** 的芯片成功率。
- 系统级封装 (SiP) 方法论的领先地位：为倒装芯片 PMIC 和 SiP 集成建立了端到端设计方法，旨在减少复杂多芯片电源传输网络的迭代周期。
- 固态电路领域成就：在 IEEE 定制电路会议 (CICC 2026) 和 IEEE 欧洲固态电路会议 (ESSERC 2026) 上以第一作者身份发表了 **3** 篇旗舰会议论文。在顶级期刊 IEEE 固态电路杂志 (JSSC) 上以第一作者身份发表了 **2** 篇常规论文，重点关注先进的 IVR 架构。

第二支柱：高效功率转换和智能混合信号控制

- 架构和拓扑突破：研发了多种新型混合/谐振开关电容 (SC) 拓扑和基于轨迹的软开关控制技术，不断拓宽 3D 功率密度和系统效率的帕累托前沿。
- 专用领域电源管理：率先将轻量级学习算法应用于 SIMO 转换器控制的芯片实现，在异构 SoC 中实现动态、实时交叉调节缓解。
- 电力电子领域成就：在顶级会议上发表了 **6** 篇第一作者论文，包括 IEEE 应用电力电子会议及展览会 (APEC) 和 IEEE 电力电子控制与建模研讨会 (COMPEL)，证明了在高密度功率转换领域的持续领先地位。

第三支柱：时钟功耗协同设计、动态扩展和弹性架构

- 主动式功率性能扩展：率先开展指令驱动的主动式时钟和自适应电源管理研究，实现了显著的节能和超动态瞬态响应。
- 统一电源和时钟调节：开创性地设计了用于高能效计算的统一电压和频率调节器 (UVFR)，弥合了数字时钟和模拟电源输送之间的设计鸿沟。
- 电路与系统领域成就：发表了 **4** 篇第一作者论文，其中包括在 IEEE 电路与系统汇刊 I (TCAS-I) 和 IEEE 亚洲固态电路会议 (A-SSCC 2022) 上发表了一篇常规论文。

荣誉与学术服务

2026 **分会主席** – *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*

2026 期刊审稿人 – *IEEE Transactions on Power Electronics (TPEL)*

2023-2025 **项目负责人** – 北京市自然科学基金青年项目 (Grant No. 4244106)

2023-2026 主要参与人 – 国家自然科学基金面上项目 (Grant No. 62374100)

2023-2026 主要参与人 – 国家重点研发计划青年科学家项目 (Grant No. 2022YFB4401100)

2026 主要参与人 – 北京信息科学与技术国家研究中心 (Grant No. BNR2026RC01013)

2023-2026 国家海外博士后人才引进计划

2023-2026 “水木学者“人才计划（海外）

职业经历

博士后研究员	**2026-Present**	香港科技大学及功率半导体与应用中心 (**PowerSAC**)
博士后研究员	**2023-2026**	清华大学集成电路学院
助理研究员	**2023-2026**	清华大学集成电路学院
助教	**2018-2023**	香港科技大学电子及计算机工程学院